a source driver for supplying video signals to 2n source signal lines S1, S2, ···, Sn, Sn+1, Sn+2, ···, S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···, GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···, GmR, wherein:

the pixels connected to the source signal lines S1, S2, ···, S2n are supplied with the selection signals from the first gate signal lines G1L, G2L, ···, GmL;

the pixels connected to the source signal lines Sn+1, SN+2, ···, S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, ···, GmR;

the selection signal starts to be supplied to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

the selection signal starts to be supplied to the first gate signal line G2L while the selection signal is supplied to the second gate signal G1R.

24. (Amended) A method of driving an active matrix display device comprising:

a pixel portion in which (m x 2n) pixels, each including at least one TFT, are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, ···, Sn, Sn+1, Sn+2, ···, S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···, GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···, GmR, wherein said method comprises the steps of:

supplying the pixels connected to the source signal lines S1, S2, ···, Sn with the selection signals from the first gate lines G1L, G2L, ···, GmL;

supplying the pixels connected to the source signal lines Sn+1, Sn+2, ···, S2n with the selection signals from the second gate lines G1R, G2R, ···, GmR; and

sequentially supplying the selection signals to the first gate signal line G1L, the second gate signal line G1R, the first gate signal line G2L, the second gate signal line G2R, ···, the first gate signal line GmL, and the second gate signal line GmR in this order with a delay of a half period between the respective adjacent gate signal lines.

Please add the following new claims:

25. (New) A display device comprising:

a pixel portion in which (m x 2n) pixels, each including at least one TFT, are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, ···, Sn, Sn+1, Sn+2, ···, S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···, GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···, GmR, wherein:

the pixels connected to the source signal lines S1, S2, ···, Sn are supplied with the selection signals from the first gate signal lines G1L, G2L, ···, GmL;

the pixels connected to the source signal lines Sn+1, SN+2, ···, S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, ···, GmR;

the selection signal starts to be supplied to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

the selection signal starts to be supplied to the first gate signal line G2L while the selection signal is supplied to the second gate signal line G1R,

wherein the m first gate signal lines G1L, G2L, ···, GmL of the first gate driver are not connected to the m second gate signal lines G1R, G2R, ···, GmR of the second gate driver.

26. (New) A display device comprising:

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a pixel portion in which (m x 2n) pixels, each including at least one TFT, are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, ···, Sn, Sn+1, Sn+2, ···, S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ···GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ···, GmR, wherein:

the pixels connected to the source signal lines S1, S2, ···, Sn are supplied with the selection signals from the first gate signal lines G1L, G2L, ···, GmL;

the pixels connected to the source signal lines Sn+1, Sn+2, ···, S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, ···, GmR;

the selection signal starts to be supplied to one of the i-th gate signal line GiL and the second gate signal line GiR while the selection signal is supplied to the other one of the first gate signal line GiL and the second gate signal line GiR.